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09/745,114	12/20/2000	Sam Yang	303.714US1	6915

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/745,114	Applicant(s) YANG, SAM	
	Examiner Scott R. Wilson	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-125* is/are pending in the application.

4a) Of the above claim(s) *33-72 and 107-109* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32,73-106 and 110-125* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-32, 73-106 and 110-125 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 1, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes.

As to claim 2, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 3, Horiike et al. discloses (col. 7, line 15) the dielectric layer to be formed from tantalum oxide.

As to claim 4, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from titanium oxide, which is understood in the art to be able to be formed with an orthorhombic crystal structure, for example as recited in Oshida, col. 5, line 38.

Claims 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 5, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

As to claim 6, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

As to claim 7, Horiike et al. discloses (col. 7, line 16) that either electrode may include tungsten.

Claim 8 is a **product-by-process claim**:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi* et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 8 does not distinguish over Horiike et al. regardless of the process used to form the buffer layer, because only the final product is relevant, and not the process of making such as *growing the buffer layer by oxidizing the one electrode*.

Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 9, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, and it is understood in the art that tungsten is a refractory metal.

As to claim 10, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

As to claim 11, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

Claims 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 12, Horiike et al., Figure 2, discloses a vertical capacitor comprising a bottom electrode (15), a top electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the bottom electrode and the top electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and the bottom electrode.

As to claim 13, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 14, Horiike et al. discloses (col. 7, line 15) the dielectric layer to be formed from tantalum oxide.

As to claim 15, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from titanium oxide, which is understood in the art to be able to be formed with an orthorhombic crystal structure, for example as recited in Oshida, col. 5, line 38.

Claims 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 16, Horiike et al., Figure 2, discloses a capacitor comprising a bottom electrode (15), a top electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the bottom electrode and the top electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and the bottom electrode. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, and it is understood in the art that tungsten is a refractory metal.

As to claim 17, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

As to claim 18, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and it is understood in the art that tungsten is a refractory metal.

As to claim 19, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride.

Claims 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 20, Horiike et al., Figure 2, discloses a capacitor comprising a bottom electrode (15), a top electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the bottom electrode and the top electrode and a buffer layer (lower layer 17), which may be formed

from a metal oxide (col. 7, line 11), intermediate the dielectric layer and the bottom electrode. Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 21, Horiike et al. discloses (col. 7, line 15) the dielectric layer to be formed from tantalum oxide.

As to claim 22, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claims 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 23, Horiike et al., Figure 2, discloses a capacitor comprising a bottom electrode (15), a top electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the bottom electrode and the top electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and the bottom electrode. Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 24, Horiike et al. discloses (col. 7, line 15) the dielectric layer to be formed from tantalum oxide.

Claim 25 is rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. Horiike et al., Figure 2, discloses a capacitor comprising a bottom electrode (15), a top electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the bottom electrode and the top electrode and a buffer layer (lower layer 17), which may be formed from a

metal oxide (col. 7, line 11), intermediate the dielectric layer and the bottom electrode. Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Horiike et al. further discloses (col. 7, line 15) the dielectric layer to be formed from tantalum oxide.

Claims 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 26, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

As to claim 27, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

Claims 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. Claim 28 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*. As to the teaching regarding claim 28, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer

17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes.

As to claim 29, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claims 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. As to claim 30, Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much less than 300.

As to claim 31, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 32, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

Claim 106 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer or the bottom electrode, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer or annealing the bottom electrode*.

Claim 106 is rejected under 35 U.S.C. 102(b) as being anticipated by Horiike et al.. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and

an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 73.

Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal

oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 74.

Claim 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed

from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 75.

Claim 76 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the

art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 76.

Claim 77 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*.

Claims 77 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. As to claim 77, Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be

formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 77.

Claim 78 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer at a temperature of at least 700 degrees Celsius*.

As to claim 78, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode

(18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 79.

Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Horiike et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode

(18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much less than 300. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Ino to obtain the invention as specified in claim 80.

Claims 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. As to claim 81, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed

between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 81.

As to claim 82, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric

layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 83.

Claim 84 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second

electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 84.

Claim 85 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a

second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 85.

Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second

electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much less than 300. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 86.

Claim 87 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*.

Claim 87 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the

array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 87.

Claims 88 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Horiike et al.. As to claim 88, Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to

the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Chu et al. to obtain the invention as specified in claim 88.

As to claim 89, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 90 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Horiike et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of

the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Chu et al. to obtain the invention as specified in claim 90.

Claim 91 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Horiike et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much

less than 300. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Chu et al. to obtain the invention as specified in claim 91.

Claim 92 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Horiike et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11),

intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Chu et al. to obtain the invention as specified in claim 92.

Claim 93 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*.

Claim 93 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Horiike et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit

coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Chu et al. to obtain the invention as specified in claim 93.

Claims 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. As to claim 94, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column

access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 94.

As to claim 95, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 96 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of

memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 96.

Claim 97 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory

comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 97.

Claim 98 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much less than 300. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The

motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 98.

Claim 99 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*.

Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the

time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 99.

Claims 100 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. As to claim 100, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7,

line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 100.

As to claim 101, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 102 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first

electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 102.

Claim 103 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between

the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide. Although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 103.

Claim 104 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address

decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. Horiike et al. also discloses (col. 7, line 12) that the dielectric layer may be formed from a lamination of titanium oxide (upper layer 17) and tantalum pentoxide (16). The dielectric constant of tungsten trioxide is 300, while the dielectric constants of titanium oxide and tantalum pentoxide are 86 and 30, respectively, both of which are much less than 300. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 104.

Claim 105 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *annealing the metal oxide buffer layer*.

Claim 105 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high

dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 105.

Claims 110-112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. As to claim 110, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7).

Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 110.

As to claim 111, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 112, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

Claims 113-115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. As to claim 113, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide

(col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 113.

As to claim 114, Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 115 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *oxidizing the one electrode*.

As to claim 115, Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claims 116 and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Horiike et al.. As to claim 116, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access

circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, and it is understood in the art that tungsten is a refractory metal. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Yoneda to obtain the invention as specified in claim 116.

As to claim 117, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

Claims 118-120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. As to claim 118, Le et al., Figure 1, discloses a memory system

comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 118.

As to claim 119, Horiike et al. discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

As to claim 120, although not explicitly stated in Horiike et al., it is understood in the art that tungsten oxide may be formed with an orthorhombic crystal structure, for example, as recited in Li et al., col. 2, line 62.

Claims 121-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. As to claim 121, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second

electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide, also referred to in the art as tungsten trioxide. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 121.

As to claim 122, Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 123 is a **product-by-process claim** and does not distinguish over Horiike et al. regardless of the process used to form the metal oxide buffer layer, because only the final product is relevant, and not the process of making such as *oxidizing the one electrode*.

As to claim 123, Horiike et al. further discloses (col. 7, line 16) that either electrode may be formed from tungsten nitride and that (col. 7, line 12) the buffer layer may be formed from tungsten oxide.

Claim 124 and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Horiike et al.. As to claim 124, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114)

coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode. Horiike et al., Figure 2, discloses a capacitor comprising a first electrode (15), a second electrode (18), a dielectric layer (upper layer 17 laminated with 16) interposed between the first electrode and the second electrode and a buffer layer (lower layer 17), which may be formed from a metal oxide (col. 7, line 11), intermediate the dielectric layer and one of the first and second electrodes. Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide, and it is understood in the art that tungsten is a refractory metal. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory system of Le et al. with the capacitor of Horiike et al.. The motivation for doing so would have been form a capacitor with high dielectric constant, rather than a capacitor with increased surface area, which would have complicated structures (Horiike et al., col. 2, line 7). Therefore, it would have been obvious to combine Horiike et al. with Le et al. to obtain the invention as specified in claim 124.

As to claim 125, Horiike et al. discloses (col. 7, line 12) that the buffer layer may be formed from tungsten oxide.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

srw
August 22, 2002

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